# Nonvolatile and SDRAM Ferroelectric Memories for Space Applications

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## Abstract

A ferroelectric memory cell has been designed for use in memory designs that are hardened to total ionizing dose and single event upset using hardened by design techniques. This approach allows fabrication of the memories at a commercial semiconductor vendor. The memory cell is being used in two prototype designs.

A 1-kbit ferroelectric memory prototype has been designed to provide a test vehicle for evaluating radiation hardened nonvolatile ferroelectric memories for radiation tolerance and reliability. The intent is to demonstrate the technology and design methodologies at lower cost on the test vehicle prior to designing and producing a radiation hardened 4 Mbit nonvolatile ferroelectric memory. The test vehicle design provides flexibility for varying the operation of the memory array and for enhanced testability.

A 4-Mbit synchronous DRAM (SDRAM) ferroelectric memory has been designed to provide an intermediate solution for both nonvolatile and volatile RAMs. By operating the ferroelectric memory at lower programming voltages than used for nonvolatile ferroelectric memories, retention can be traded off against endurance to provide high levels of endurance. Retention is anticipated to be at least one day and endurance is expected to be at least $10^{12}$. Both prototype products are targeted for broad space applications, including potentially the JPL X2000 program.

Fujitsu, a semiconductor company that is supplying commercial products incorporating ferroelectric memory, is performing the wafer fabrication at 0.35 micron design rules. First silicon on both prototype products is expected to be received around the time of the Symposium.

Radiation hardened volatile and nonvolatile ferroelectric memories are targeted for space applications because the inherent radiation hardness can be orders of magnitude better than Flash memory with no need for heavy shielding. In addition to superior radiation hardness, the ferroelectric memory provides very fast programming times, very high endurance, and low power operation ideal for space applications.

Previous work has shown ferroelectric capacitors for use in ferroelectric memories are resistant to ionizing radiation and neutron exposure. Previous work has also shown ferroelectric memories are resistant to SEU events and proton irradiation under unbiased conditions. However, meaningful evaluation of the response of ferroelectric memories to SEU events and proton irradiation under bias was not possible because the CMOS circuitry was not radiation hardened. The ferroelectric memories of this program will enable the response of ferroelectric memory to be evaluated under bias for all four types of radiation exposures.

Radiation hardness of ferroelectric technology will be reviewed. A description of the architecture and operation of the ferroelectric memory cell will be presented for both designs. Planned timetables for the products will be presented as well as anticipated specifications.

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